CLOCK DIVIDER AND CLOCK DIVIDING METHOD FOR A DLL CIRCUIT

BACKGROUND OF THE INVENTION

5   Field of the invention

The present invention relates to a DLL (Delay Lock Loop) circuit, and more particularly to a clock divider and a clock dividing method for a DLL circuit which can reduce a power consumption when a synchronous memory device is kept in a

10   power-down mode that corresponds to a low power consumption state.

Description of the Prior Art

As generally known in the art, in a synchronous memory

15   device (hereinafter referred to as a memory device), an internal clock signal is used in order to adjust an operation timing of the memory device and to prevent malfunction of the memory device. In the case that an externally inputted clock is used inside a typical memory device, a time delay occurs.

20   A DLL (Delay Lock Loop) circuit is a circuit which synchronizes a phase of an internal clock of the memory device with a phase of the externally inputted clock in order to control such a time delay.

FIG. 1 is a block diagram of a general DLL circuit.

As illustrated in FIG. 1, the DLL circuit includes a clock buffer unit 100 for receiving an external clock signal, a clock divider 110 for dividing an output signal of the clock buffer unit 100, a delay unit 130 and a delay model 150 for delaying an output signal of the clock divider 110 for a predetermined time, a phase comparator 120 for comparing a phase of an output signal of the delay model 150 with a phase of the output signal of the clock divider 110, and a DLL signal driving unit 140 for receiving output signals of the delay unit 130 and outputting an internal clock signal used in the memory device.

Clock buffers 101 and 102 of the clock buffer unit 100 are buffer circuits that convert a potential level of the externally inputted clock signals CLK and /CLK into a potential level used inside the memory device. Generally, the clock buffers of the memory device are activated by a clock enable signal CKE (not illustrated).

The clock divider 110 receives and divides the output signal Rise_clk of the clock buffer 102. The clock divider 110 divides the frequency of the clock signal Rise_clk into $1/2^M$ (here, M is the number of dividers), and outputs two output signals S2 and S3. The output signal S2 is an inverted signal of the output signal S3. The output signal S2 of the clock divider 110 is applied to the phase comparator 120

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after being delayed for a predetermined time through a third delay line and the delay model 150. For reference, the delay model 150 is a dummy delay unit for compensating for a phase difference between the output signal S3 and an output signal

5   (i.e., feedback signal).

The phase comparator 70 compares the phase of the output signal S3 of the clock divider with the phase of the output signal (i.e., feedback signal) of the delay model 150, and reduces the time difference between the two output signals.

10   The output signal of the phase comparator 120 is applied to a shift controller of the delay unit. If the phase difference is 0, the shift controller outputs a DLL_lockb signal so that a shift register maintains its present state. On the contrary, if there exists any phase difference, the

15   shift controller controls the shift register to adjust a delay time of the third delay line. An output signal SR of the shift controller makes the shift register shift to the right, and another output signal SL of the shift controller makes the shift register shift to the left. First and second

20   delay lines delay output signals Rise_clk and Fall_clk of the clock buffers 101 and 102 for a predetermined time under the control of the shift controller, and provide corresponding output signals, i.e., an input rising clock irclk and an input falling clock ifclk. The first to third delay lines are

composed of a logic circuit having a very short delay time to reduce a jitter.

The first and second DLL signal drivers of the DLL signal driving unit 140 are buffers for providing DLL clock signals used in the memory device. Accordingly, output signals, i.e., a rising clock_dll rclk_dll and a falling clock_dll fclk_dll, of the first and second DLL signal drivers 140 are used as the internal clock signals.

The DLL circuit compensates for the time difference between the externally inputted clock signal CLK and the internal clock signal. Accordingly, the output signals, i.e., the rising clock_dll rclk_dll and the falling clock_dll fclk_dll, of the first and second DLL signal drivers, which are the internal clock signals of the memory device, are synchronized with the external clock CLK through the DLL circuit.

FIG. 2 illustrates a circuit diagram of the clock divider illustrated in FIG. 1.

The clock divider 110 includes first to third dividers 200, 201 and 220, which are connected in series. That is, an output signal of the first divider 200 is applied to an input terminal of the second divider 210, and an output signal of the second divider is applied to an input terminal of the third divider 220. In FIG. 2, the signal S1 corresponds to

the signal Rise_clk in FIG. 1, and the signal S2 is an inverted signal of the signal S3.

The first divider outputs a clock signal A, which is obtained by dividing the frequency of the clock input signal S1 into 1/2. The second divider outputs a clock signal B, which is obtained by dividing the frequency of the output signal A of the first divider into 1/2. Accordingly, the frequency of the output signal B of the second divider is 1/4 of the frequency of the clock input signal S1. The third divider outputs a clock signal C, which is obtained by dividing the frequency of the output signal B of the second divider into 1/2. Accordingly, the frequency of the output signal C of the third divider is 1/8 of the frequency of the clock input signal S1. This clock divider is called a 1/8-clock divider. As shown in FIG. 3, the duty rates of the output signals of the first to third dividers are not identical, but the duty rates can be modified if needed.

The respective divider circuit of FIG. 2 is composed of NAND gates, but many modifications thereof can be made by those skilled in the art.

FIG. 3 is a timing diagram of the clock divider illustrated in FIG. 2.

As show in FIG. 3, the period of the clock signal S1 applied to the first divider is tCK. The frequency of the

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output signal A of the first divider is 1/2 of the frequency of the clock signal S1, and the width of the high-level pulse signal is the same as the period of the clock signal S1. Also, the 1/8-clock divider outputs an output signal S2 of 5 which the width of a low-level pulse signal is tCK. As show in FIG. 3, the output signals S2 and S3 of the conventional clock divider are not controlled by an externally inputted clock enable signal CKE, and thus they are processed irrespective of the state of the memory device. Accordingly, 10 even in the case of a power-down mode in which the power consumption of the memory device is reduced, the output waveform of the clock divider becomes the same as that in a non-power-down mode of the memory device. For this reason, the DLL circuit consumes the same amount of current as that 15 in the non-power-down mode even though the memory device is in the power-down mode.

Generally, in the case that the memory device is in the power-down mode, the power supply of the memory device is stabilized. Thus, it does not cause big problem even if the 20 number of times of phase comparison is reduced in the power-down mode in comparison to that in the non-power-down mode.

As described above, the conventional DLL circuit has the drawbacks that even if the memory device is in the power-down mode, the DLL circuit generates the internal clock signal,

which is to be used inside the memory device, in the same manner as in the non-power-down mode, and this causes an unnecessary current consumption.

5   SUMMARY OF THE INVENTION

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a
10 clock divider for a DLL circuit which can reduce the power consumption by reducing the number of times of phase comparison in the DLL circuit when a memory device is in a power-down mode.

In order to accomplish this object, there is provided a
15 clock divider for a DLL (Delay Lock Loop) circuit which can reduce the number of times of phase comparison in a phase comparator by dividing an external input clock into $1/2^{(M-1)}$ (where, M is the number of dividers) in the case that a memory device is in a non-power-down mode and by dividing the
20 external input clock into $1/2^{M}$ in the case that the memory device is in a power-down mode.

In one aspect of the present invention, there is provided a clock divider for a DLL circuit comprising M dividers connected in series, and a power-down controller for

receiving an output signal of the (M-1)-th divider and an output signal of the M-th divider and selectively outputting the output signals, wherein the respective dividers divide a frequency of a clock signal inputted to the respective

5 dividers into 1/2, and the output signal of the power-down controller has a frequency obtained by dividing the frequency of the clock signal inputted to the first divider into $1/2^M$ or $1/2^{(M-1)}$ in accordance with a logic level of a control signal.

In the present invention, if the logic level of the

10 control signal is a first state (high level), the output signal of the power-down controller becomes the output of the (M-1)-th divider, and if the logic level of the control signal is a second state (low level), the output signal of the power-down controller becomes the output of the M-th

15 divider.

In the present invention, a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the first divider, and a pulse width of a low-level state of output signals of the

20 second to M-th dividers is the same as the period of the input signal of the first divider.

In another aspect of the present invention, there is provided a clock dividing method for a DLL circuit of a synchronous memory device for synchronization of an external

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input clock with an internal input clock, the method comprising the steps of selectively outputting an output signal of a (M-1)-th divider and an output signal of an M-th divider among M dividers, connected in series, for

5 respectively dividing a frequency of the input clock signal into 1/2.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a general DLL circuit;

15 FIG. 2 is a circuit diagram of a clock divider illustrated in FIG. 1;

FIG. 3 is a timing diagram of the clock divider illustrated in FIG. 2;

FIG. 4 is a circuit diagram of a clock divider according

20 to the present invention; and

FIG. 5 is a timing diagram of the clock divider illustrated in FIG. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. In the following description and

5 drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description on the same or similar components will be omitted.

FIG. 4 is a circuit diagram of a clock divider according

10 to the present invention.

As illustrated in FIG. 4, the clock divider for a DLL circuit according to the present invention includes first to fourth dividers 400, 410, 420 and 430 and a power-down controller 500.

15 The first to fourth dividers have the same construction using NAND gates. For reference, diverse modifications of the clock divider can be made by those skilled in the art.

As shown in FIGs. 4 and 5, the first divider 400 divides an input signal S1, and outputs a clock signal A having a

20 frequency that is 1/2 of the frequency of the input signal. That is, the period of the output clock signal of the first divider is twice the period of the input clock signal of the first divider. Accordingly, the pulse width of the high-level state of the output signal of the first divider is the same

as the period of the input clock signal of the first divider.

The second divider 410 divides the input clock signal A, and outputs a clock signal B having a frequency that is 1/2 of the frequency of the input clock signal. That is, the

5 period of the output clock signal of the second divider is twice the period of the input clock signal of the second divider. As illustrated in FIGs. 4 and 5, the pulse width of the low-level state of the output signal of the second divider is the same as the period of the input clock signal

10 of the first divider.

The third divider 420 divides the input clock signal B, and outputs a clock signal C having a frequency that is 1/2 of the frequency of the input clock signal. That is, the period of the output clock signal of the third divider is

15 twice the period of the input clock signal of the third divider. As illustrated in FIGs. 4 and 5, the pulse width of the low-level state of the output signal of the third divider is the same as the period of the input clock signal of the first divider.

20 The fourth divider 430 divides the input clock signal C, and outputs a clock signal D having a frequency that is 1/2 of the frequency of the input clock signal. That is, the period of the output clock signal of the fourth divider is twice the period of the input clock signal of the fourth

divider. As illustrated in FIGs. 4 and 5, the pulse width of the low-level state of the output signal of the fourth divider is the same as the period of the input clock signal of the first divider.

5   The power-down controller 500 receives the output clock signals of the third and fourth dividers 420 and 430, and selects and outputs one of the output clock signals of the third and fourth dividers according to the logic level of the clock enable signal CKE that is the control signal.

10   An example of the power-down controller is illustrated in FIG. 4. As illustrated, the power-down controller comprises two transmission gates 510 and 520. Each transmission gate is composed of a PMOS transistor and an NMOS transistor connected in parallel. The on/off operation

15 of the transmission gate is controlled by the clock enable signal CKE. If one transmission gate is turned on, the other transmission gate is turned off. As illustrated in FIG. 4, the output clock signal of the third divider is applied to the transmission gate 510, and the output clock signal of the

20 fourth divider is applied to the transmission gate 520. If the clock enable signal CKE that is the control signal is in a high level, the transmission gate 510 is turned on, and if the clock enable signal CKE is in a low level, the transmission gate 520 is turned on. Accordingly, in the case

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that the clock enable signal CKE is in the high level, the waveform of the output signal S3 of the power-down controller is the same as the waveform of the output clock signal C of the third divider. In the case that the clock enable signal

5   CKE is in the low level, the waveform of the output signal S3 of the power-down controller is the same as the waveform of the output clock signal D of the fourth divider.

In the embodiment of the present invention, the clock divider comprises four dividers and a power-down controller.

10   However, the number of dividers may be increased to more than 5, or may be decreased to 2 or 3 as needed.

As described above, the clock divider for a DLL circuit according to the present invention can selectively output one of the output clock signal C of the third divider and the

15   output clock signal D of the fourth divider according to the clock enable signal that is the control signal. Accordingly, by applying the clock divider according to the present invention to a DLL circuit, the output signal of the third divider is selected in the same manner as the conventional

20   clock divider in the case that the memory device is in the non-power-down mode, but the output signal of the fourth divider is selected in the case that the memory device is in the power-down mode in which the power consumption of the memory device is reduced, thereby reducing the current loss

of the DLL circuit.

Although preferred embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.